Ultra-Low Latency Packet Buffering Engine Factsheet: Packet Buffer Memory Size Allocation

ULTRA-LOW LATENCY PACKET BUFFERING ENGINE FACTSHEET: PACKET BUFFER MEMORY SIZE ALLOCATION

EXECUTIVE SUMMARY

This document provides a detailed technical overview of packet buffer memory size allocation within the next-generation carrier-grade forwarding engine. Proper buffer memory dimensioning directly determines the device’s ability to absorb micro-bursts, maintain line-rate throughput under congestion, and guarantee Quality of Service (QoS) for latency-sensitive traffic. This datasheet covers architectural principles, dynamic allocation policies, hardware specifications, and ordering information for platforms utilizing shared, hierarchical, and per-port buffer memory models.



HARDWARE ARCHITECTURE & SILICON

The packet buffering subsystem is integrated directly into the forwarding ASIC, employing a true shared-memory architecture. Unlike static per-port partitioning, this model dynamically allocates buffer blocks from a global pool to ports experiencing congestion. The memory controller operates at line rate, supporting simultaneous read/write operations across all interfaces without head-of-line blocking. Key internal components include:

- Central Buffer Manager (CBM): Tracks free buffer cell addresses and enforces allocation thresholds.

- Dynamic Threshold Logic: Automatically adjusts maximum queue lengths based on active port counts and available memory.

- Low-Latency Cut-Through Path: Bypasses buffer write for forwarding decisions made within 64 bytes of frame reception.

For deep buffer configurations, external high-density DRAM (DDR4/DDR5) is accessible via a dedicated memory bus, providing up to 32 GB of additional burst absorption capacity.

KEY FEATURES & ROUTING LOGIC

- Per-Queue Dynamic Thresholds: Four configurable congestion avoidance thresholds (minimum, low, medium, high) per hardware queue.
- Ingress and Egress Buffer Partitioning: Separate memory pools for ingress and egress, with capacity to reassign under-utilized ingress space to egress during sustained downstream congestion.
- Microburst Absorption: Dedicated reserve of 2 MB per 10 Gb/s port for 1 ms bursts at full line rate without packet loss.
- Priority Flow Control (PFC) Autoconfiguration: PFC thresholds are automatically derived from current buffer occupancy and link speed.
- Packet Shaper Integration: Buffer threshold exceedance triggers hardware-based traffic shaper per egress queue.
- Lossless vs. Lossy Queue Modes: Admin-selectable mode per VLAN or port; lossless queues lock minimum buffer residency.

COMPLIANCE & STANDARDS

- IEEE 802.1Qbb – Priority-based Flow Control

- IEEE 802.1Qaz – Enhanced Transmission Selection (ETS)

- RFC 2814 – Integrated Services over Specific Link Layers

- MEF 10.3 – Service Level Specification compliance for burst handling

- RoCEv2 Congestion Control interoperability

TECHNICAL SPECIFICATIONS

Total Shared Packet Buffer: 64 MB (on-chip SRAM) / Expandable to 32 GB (off-chip DDR4 optional)

Per-Port Dynamic Buffer Limit: Up to 100% of global pool when thresholds permit

Minimum Reserved Buffer per Queue: 32 KB (configurable)

Maximum Queue Depth: 32,768 packets (dependent on MTU)

Latency Added by Buffer Write/Read: < 400 ns (cut-through bypass) / 1.2 µs (store-and-forward, 64B frame)

Allocation Granularity: 256-byte buffer cells

Congestion Thresholds: 4 levels (25%, 50%, 75%, 90% occupancy)

Parameter	**Specification**
Form Factor	1RU Standalone / 2RU Expandable Chassis
Switching Capacity	2.56 Tbps (non-blocking, all packet

	sizes)
Power Supply	Dual Hot-Swappable Redundant AC/DC (100-240V / -48V DC)
Buffer Architecture	Shared memory, dynamic thresholds, cut-through/store-and-forward selectable per port
Max Buffer per Port (dynamic)	Up to 100% of global pool (subject to policy)
Operating Temperature	0°C to 45°C (ambient)
MTBF (predicted)	320,000 hours (Telcordia SR-332)

ORDERING SKU INFORMATION

Base SKU: PB-64G-SFP – 64 GB total buffer capacity (external DRAM), SFP+ interfaces, no on-chip SRAM expansion

PB-128G-Q28 – 128 GB buffer, 25/100 GbE ports, includes on-chip 64 MB + external DRAM

PB-32M-LC – 32 MB on-chip only, low latency cut-through optimized, 1 GbE/10 GbE access

PB-DLB-CUST – Customer-specific buffer sizing, 32 MB to 256 GB, contact engineering for deep buffer profiles

All SKUs include per-queue dynamic threshold firmware license. Optional advanced buffer analytics license (PB-ANALYTICS) provides real-time occupancy heatmaps and burst anomaly detection.

